Instruction manual

DATA I/O

Programming systems for tomorrow... today

PROM PROGRAMMER
Program Card Set
909/919-1226-1

025-1226-1 REV L NOV 78

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SECTION 1
SPECIFICATIONS

1.1 INTRODUCTION

Data I/O Program Card Sets configure the programmer for the requirements of particular devices. This card set, used with the appropriate socket adapter, will program and read the devices listed in Table 1-1. New applications are developed frequently; therefore, consult the most recent Data I/O Comparison Chart of Programmable Devices to supplement Table 1-1.

Table 1-1. Applications of the Program Card Set

Array Size and Technology	PROM Part Number	Programmed Logic Level	Pinout	Socket Adapter
MONOLITHIC MEMORIES				
32x8 FL	5330/6330	VOL OC	16 PIN	1046
32x8 FL	5331/6331	VOL TS	16 PIN	1046
256x4 FL	5300/6300	VOL OC	16 PIN	1035-1
256x4 FL	5301/6301	VOL TS	16 PIN	1035-1
256x8 FL	5335/6335	VOL OC	24 PIN	1033-1
256x8 FL	5336/6336	VOL TS	24 PIN	1033-1
256x8 FL	5308/6308	VOL OC	20 PIN	1028-1
256x8 FL	5309/6309	VOL TS	20 PIN	1028-1
256x8 FL	53134/63134	VOL OC	24 PIN	1115-1
256x8 FL	53135/63135	VOL TS	24 PIN	1115-1
512x4 FL	5305/6305	VOL OC	16 PIN	1035-2
512x4 FL	5306/6306	VOL TS	16 PIN	1035-2
512x8 FL	53137/63137	VOL TS	24 PIN	1115-2
512x8 FL	53141/63141	VOL TS	24 PIN	1116-2
512x8 FL	5340/6340	VOL OC	24 PIN	1033-2
512x8 FL	5341/6341	VOL TS	24 PIN	1033-2
512x8 FL	5348/6348	VOL OC	20 PIN	1064
512x8 FL	5349/6349	VOL TS	20 PIN	1064
1024x4 FL	5350/6350	VOL OC	18 PIN	1036
1024x4 FL	5351/6351	VOL TS	18 PIN	1036
1024x4 FL	5352/6352	VOL OC	18 PIN	1039-3
1024x4 FL	5353/6353	VOL TS	18 PIN	1039-3
1024x8 FL	5380/6380	VOL OC	24 PIN	1033-3
1024x8 FL	5381/6381	VOL TS	24 PIN	1033-3
1024x8 FL	5384/6384	VOL OC	24 PIN	1033-3
1024x8 FL	5385/6385	VOL TS	24 PIN	1033-3
1024x8 FL	5386/6386	VOL OC	22 PIN	1059
1024x8 FL	5387/6387	VOL TS	22 PIN	1059
RAYTHEON				
256x4 FL	29660/62	VOL OC	16 PIN	1035-1
256x4 FL	29661/63	VOL TS	16 PIN	1035-1
256x8 FL	29600	VOL OC	20 PIN	1028-1
256x8 FL	29601	VOL TS	20 PIN	1028-1
512x4 FL	29610/12	VOL OC	16 PIN	1035-2
512x4 FL	29613/14	VOL TS	16 PIN	1035-2
512x8 FL	29620/22	VOL OC	20 PIN	1064
512x8 FL	29621/23	VOL TS	20 PIN	1064
512x8 FL	29624/26	VOL OC	24 PIN	1033-2
512x8 FL	29625/27	VOL TS	24 PIN	1033-2
1024x8 FL	29630	VOL OC	24 PIN	1033-3
1024x8 FL	29631	VOL TS	24 PIN	1033-3

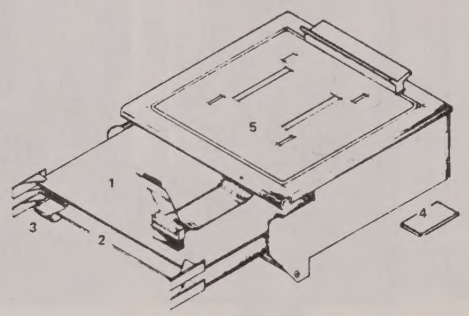
The Program Card Set includes the parts listed in Figure 1-1. The analog card produces the correct voltages in the proper waveforms for the device to be programmed or read. The digital card controls the sequences of these waveforms.

A Program Card Set for use in a System 17 or 19 Programmer is included in a Programming Pak and designated by a 919- part number. See Figure 1-1 a). A card set shipped alone, for use in a Model 1-5, 7 or 9 Programmer, bears a 909- part number. See Figure 1-1 b).

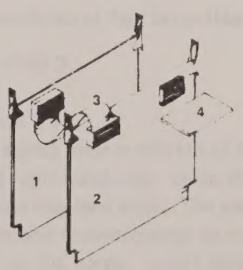
1.2 CALIBRATOR PROGRAM ADAPTER

The card set includes a Calibrator Program Adapter which mates with the Data I/O Universal Calibrator (P/N 910-1071). The PROMs on the adapter deliver the control signals to the analog card.

Using the calibrator and following the calibration procedure in Section 4 of this manual, Data I/O customers can be sure the Program Card Set remains within voltage and timing tolerances for effective programming.



a) Programming Pak for System 17 and 19 Programmers



b) Program Card Set for Model 1 - 9 Programmers

1. DIGITAL CARD	701-1225
2. ANALOG CARD	701-1226-1
3. INTERCONNECT CABLE	709-1608
4. CALIB. PROGRAM ADAPTER	910-1226-1
5. PROGRAMMING PAK CARRIER	940-0919

Figure 1-1. Parts included in the a) Programming Pak b) Program Card Set

1.3 CALIBRATION REQUIREMENTS

The need for calibration varies with the amount of use; calibration is recommended every ninety days of regular use or if programming yields fall below manufacturer's recommended minimums.

Complete calibration must be performed with a programmer that has an address and data display. Card sets for use in a Model 7 or System 17 may be properly calibrated using another Data I/O programmer. Alternately, Data I/O provides calibration service at regional Service Centers.

SECTION 2
INSTALLATION

2.1 DIGITAL CARD JUMPERS

Figure 2-1 shows the customer-selectable-jumper locations on the digital card. Refer to Table 2-1 to check the jumper positions. If a jumper change is ever made, be sure to replace the jumpers in the normal position before using the card set for programming.

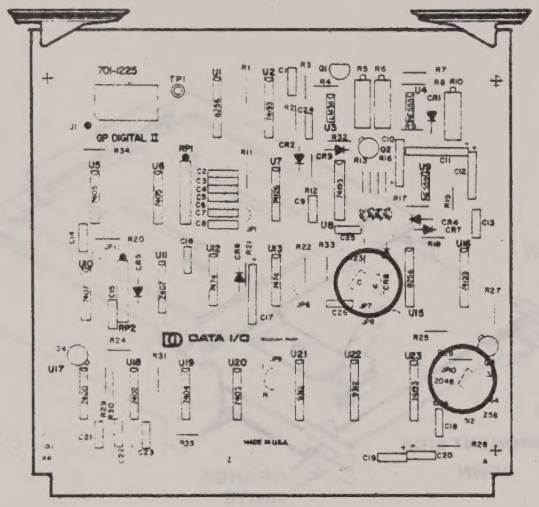


Figure 2-1. Digital Card Jumper Locations

Table 2-1. Customer - Selectable Digital Card Jumpers

JUMPER	FUNCTION	NORMAL POSITION	COMMENTS
JP 7	Reject	C	—
JP 10	Word Limit	2048	—

2.2 CARD SET INSERTION

When changing card sets in Model 1-9 Programmers, turn power OFF.

Power may remain ON when changing Programming Paks in System 17 or 19 Programmers. In this way, data may be retained in RAM during the operation.

2.2.1 MODELS 1-5

Refer to Figure 2-2.

Remove the top cover from the programmer. Each card in the card cage has color-coded extractors which correspond to the colors of the card guides. Install the analog card in the white/white position in the card cage. Install the digital card in the front brown/orange position. Components of both cards must face forward in Model 3 and 5 Programmers and to the right in Model 1 Programmers. Insert the cable into the socket receptacle, route it over the card cage, and attach it to J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

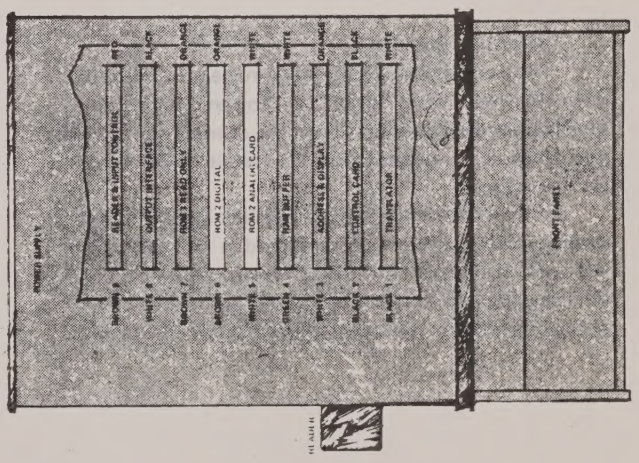


Figure 2-2. Installation of Card Set in Model 3 or 5

2.2.2 MODELS 7 AND 9

Refer to Figure 2-3.

The card set access door is located at the front of the programmer on the right-hand side. Open the door from the bottom to expose the card slots. The card guides are colored white/white and brown/orange to correspond with the extractor tabs on the cards. Insert both cards component-side-down — the analog card in the white/white slot and the digital in the brown/orange. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

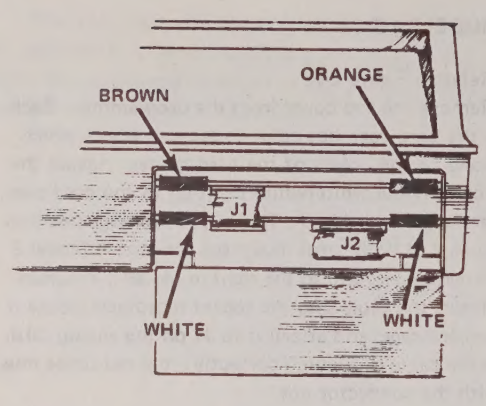


Figure 2-3. Installation of Card Set in Model 7 or 9

2.2.3 SYSTEMS 17 AND 19

Refer to Figure 2-4.

The card set should normally remain in the Programming Pak frame. Install the Programming Pak into the programmer by sliding it into the opening and lowering into position. Press gently on the handle to insure connector mating.

If the card set needs to be installed in its Programming Pak frame, insert the analog card in the white/white slot and the digital card in the brown/orange slot. With the Programming Pak face up, install both cards component-side-down. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

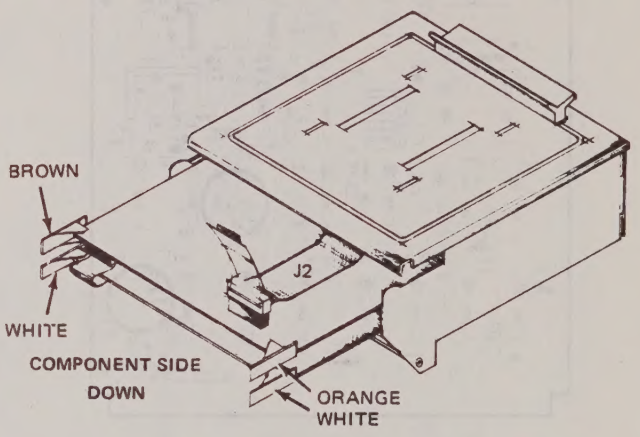


Figure 2-4. Installation of the Program Card Set in the Programming Pak

SECTION 3
OPERATION

The Program Card Set provides the link between the device in the socket adapter and the programmer's memory and control electronics. Its functions are directly controlled by the programmer. Complete instructions for operations using the card set are in the programmer instruction manual.

SECTION 4

CALIBRATION

4.1 INTRODUCTION

Calibration includes checks of power supply levels, steady-state tests of critical programming parameters, and verification of resistively loaded programming waveforms. The need for calibration varies with the amount of use, but calibration is suggested at least every ninety days. For calibration by the customer, the procedure in this section should be followed in sequence.

NOTE

If any adjustment is necessary, complete the entire calibration procedure.

4.2 TEST SET-UP

The following equipment is required to perform a calibration:

1. Data I/O Universal Calibrator, P/N 910-1071
2. Calibrator Extender Fixture:

Models 1-5	P/N 910-1136
Model 9	P/N 910-1074
System 19	P/N 910-1520

3. Digital voltmeter (DVM) — Fluke Model 8000A or equivalent.
4. A potentiometer adjustment tool
5. Dual trace oscilloscope — Tektronix 465 or equivalent
6. A jumper wire approximately 12 inches in length
7. Data I/O interconnection cables:

Models 1-5: P/N 709-1613
Model 9, System 19: P/N 709-2608, 709-1613.

To prepare for calibration of the programmer power supplies and the Program Card Set, remove the card set from the programmer and connect the Universal Calibrator according to the following instructions:

4.2.1 MODELS 1 — 5

Refer to Figure 4-1.

1. Make sure the programmer power is OFF.
2. Remove the cover from the programmer and remove the Program Card Set from the card cage.
3. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the digital card.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

4. Install the Extender Card, P/N 910-1136, (with the Universal Calibrator attached) into the programmer's analog card position (white/white). Be sure that the edge of the Extender Card is securely seated. Reinstall the digital card into the digital card position (brown/orange) in the programmer card cage.
5. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.
6. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

7. Connect the DVM ground lead to the GND test point on the Universal Calibrator.
8. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

RESET
ROM2 — ROM2
MANUAL
PROGRAM
START

4.2.2 MODEL 9

Refer to Figure 4-2.

1. Make sure the programmer power is OFF.
2. Open the Program Card Set access door from the bottom. Remove the Program Card Set.

1. ANALOG CARD
2. DIGITAL CARD
3. UNIVERSAL CALIBRATOR
4. CALIBRATOR EXTENDER FIXTURE
5. CALIBRATION PROGRAM ADAPTER
6. 26-CONDUCTOR CABLE
7. 16-CONDUCTOR CABLE

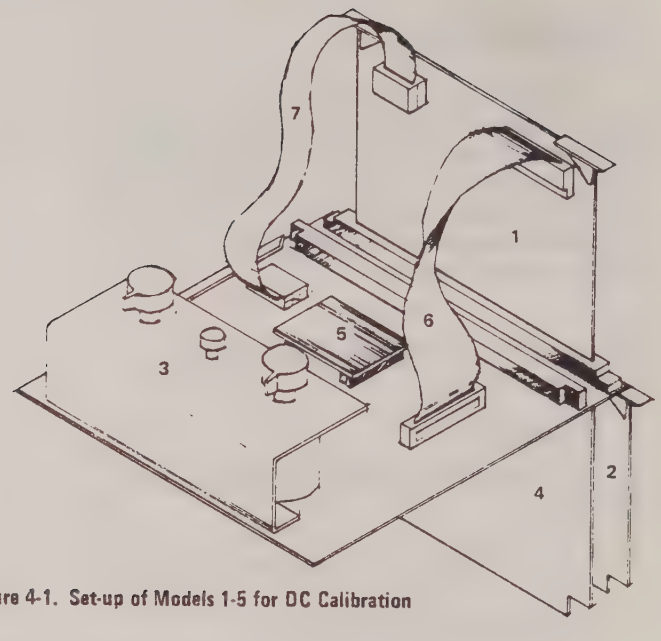


Figure 4-1. Set-up of Models 1-5 for DC Calibration

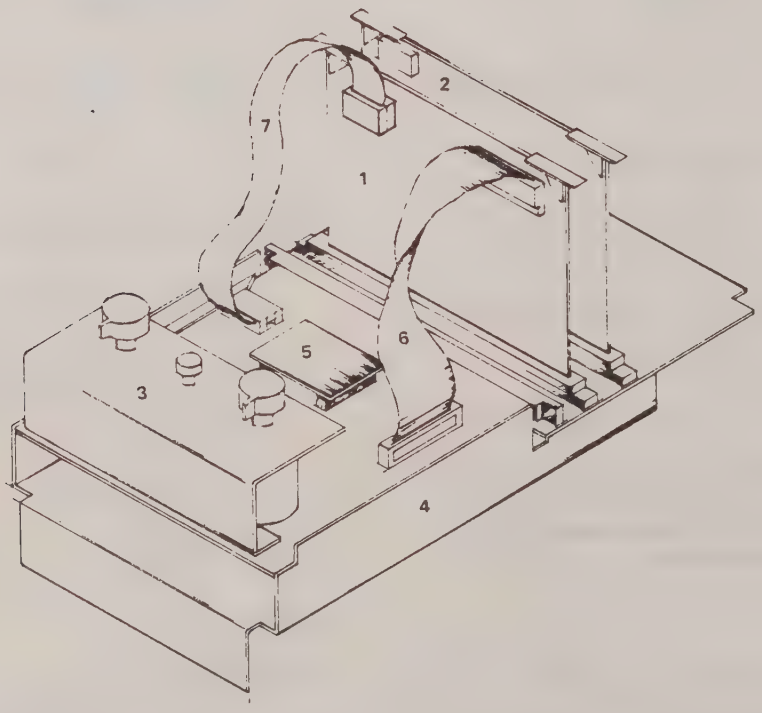
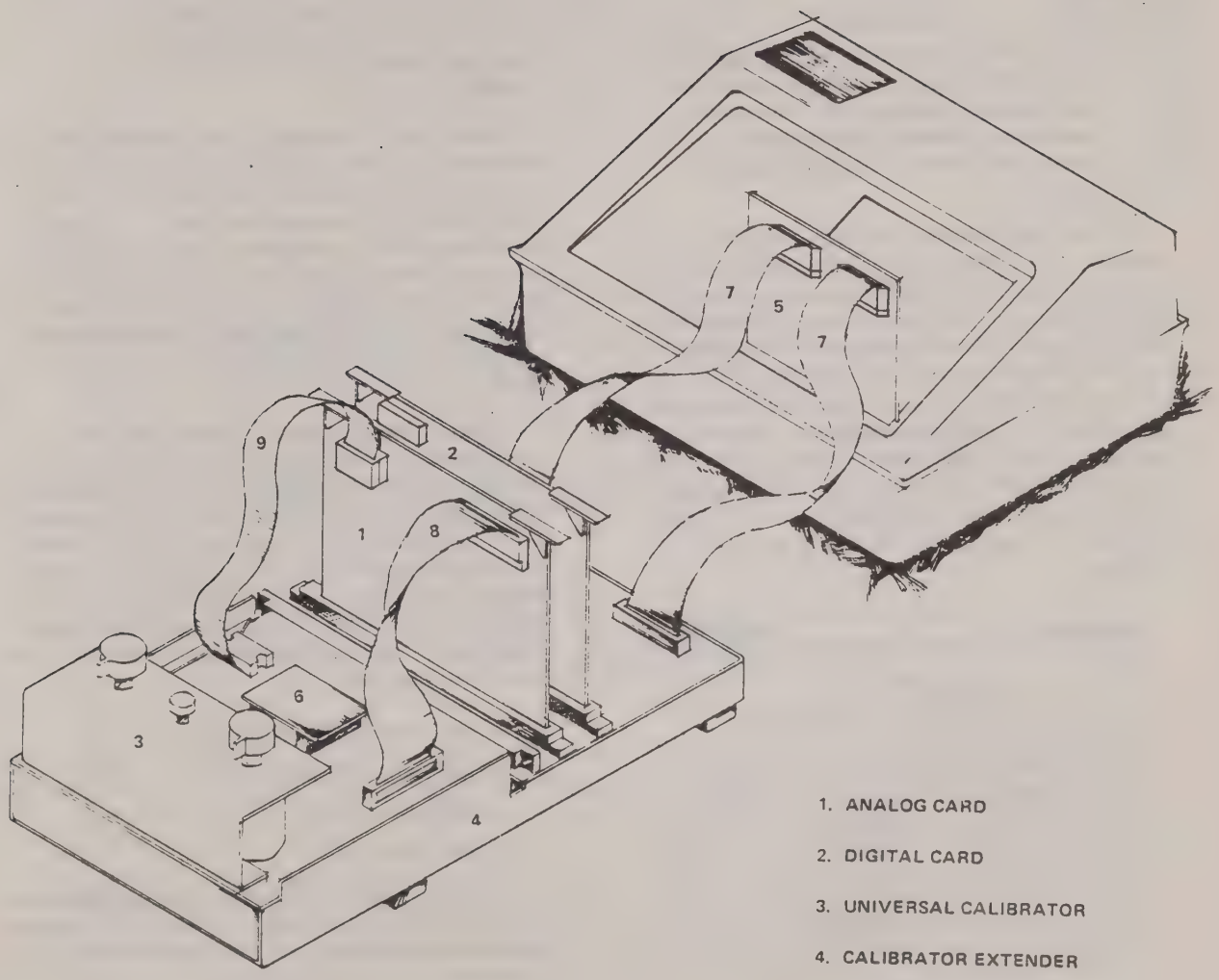


Figure 4-2. Set-up of Model 9 for DC Calibration



1. ANALOG CARD
2. DIGITAL CARD
3. UNIVERSAL CALIBRATOR
4. CALIBRATOR EXTENDER
5. CALIBRATOR INTERFACE
6. CALIBRATION PROGRAM ADAPTER
7. 50-CONDUCTOR CABLE
8. 26-CONDUCTOR CABLE
9. 16-CONDUCTOR CABLE

Figure 4-3. Set-up of System 19 for DC Calibration

● The PROGRAMMER WORD COUNT column is divided into three portions: DEC (Decimal), HEX (Hexadecimal), and OCT (Octal). When performing each step, set the address (word count) corresponding to the address number base of the programmer in use. For instance, with a programmer having a hexadecimal address readout, ignore the DEC and OCT columns.

CAUTION

DO NOT leave Word Count (address) advanced beyond 000 for extended periods. Static conditions created by the Universal Calibrator may cause thermal damage to components if the programmer is left unattended with advanced word count.

● The TEST DESCRIPTION column specifies the function to be checked in each step. In most cases, the steps simply require a DVM reading to insure that a level is within tolerance. Some steps, labeled Adjustment Steps, give a nominal (NOM) value and prescribe adjustment to that value if the level is out of the MIN-MAX range.

● The ADJUSTMENT column calls out potentiometer designations. The first four entries in the ADJ column refer to power supply potentiometers located on the power supply board of the programmer. The remaining entries in the ADJ column refer to potentiometers on the analog card. Refer to Figure 4-4 for locations of the potentiometers.

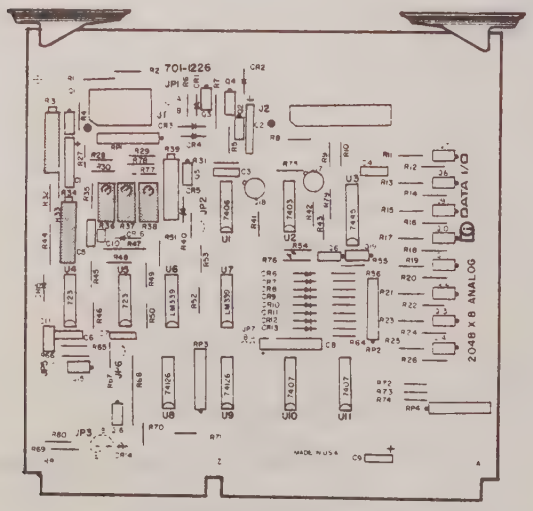


Figure 4-4. Analog Card Adjustment Locations

● The SWITCH POSITIONS column gives the switch settings for S2 and S3 on the Universal Calibrator. S2 is the load-select switch; S3 is the line-select switch. Each step on the calibration chart may require changing of switch positions. With the proper S2 and S3 positions selected, press S1 to make an accurate reading, and keep the switch depressed only long enough to complete the step.

CAUTION

DO NOT keep S1 depressed for extended periods. Certain measurements induce high programmer current levels. Extended high-current operation (S1 depressed) may damage sensitive electronic components.

● The TEST POINT column gives test point locations for the DVM probe. Most test points are located on the Universal Calibrator; some points are located on the program card. For instance, if a test point is designated as U6 P8, the DVM probe should be placed on pin 8 of integrated circuit U6 on the card indicated in the COMMENTS column.

● The LIMITS column is divided into three portions: MIN (minimum), NOM (nominal), and MAX (maximum). The values given are in volts and indicate the range into which a given DVM reading should fall. If a reading is within the limits, no adjustment is required and the programmer (or Program Card Set) passes a particular test. If a reading falls outside of the given limits, or if it cannot be adjusted to fall within the limits (in adjustment steps), the card is nonfunctional and should not be used for programming.

● The COMMENTS column on the right side of the chart provides information for certain calibration steps including call-outs of programmer operations required in some steps. The programmer provides signals to the card set on the Address bus, the Data Input bus, the START/STOP line and the FWD/REV line. The card set provides signals to the programmer on the RESET line, the VOL/VOH select line and the Data Output bus. In the course of calibration, the programmer is used to observe or set the following conditions:

- State of the START/STOP line
- State of the FWD/REV line
- Data on the DO bus
- Data on the DI bus

Key sequences for observing these conditions are given in the following paragraphs (4 3.1 – 4.3.5). Follow the tests on the Calibration Chart step-by-step, and refer to paragraphs 4.3.1 – 4.3.5 as necessary.

MODEL 9 USERS NOTE

Some of the following operations are performed differently on Model 9's with different revisions of software. Perform the following test to determine whether to refer to steps for Revision "A" software or to steps for Revision "B" or later software.

1. *Turn power OFF.*
2. *Observe the LOAD indicator while turning power ON.*
3. *If the LOAD indicator remains ON, refer to key sequences for Revision "B" or later software.*
4. *If the LOAD indicator turns OFF, refer to key sequences for Revision "A" software.*

Calibration Chart

DATA I/O
Programming systems for tomorrow...today

CALIBRATION CHART 017-1226-1 | PROGRAM CARD 909-1226-1
FIXTURE 702-1071 | MANUFACTURER MONOLITHIC MEMORIES
PROGRAM ADAPTER 910-1226-1 | PROM M. M. I. GENERIC FAMILY

DATE	REV	REVISION RECORD	DR	CK
2-77	E	C.N. #1053	KJ	DP
4-16-77	-	C.N. #1238	PW	DP
7-9-77	F	C.N. #1520 (re-typed)	GJ	
10-19-77	-	P9 update, CN #1996	GJ	GJ
11-77	-	E.C.N. #2565	FS	

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	COMMENTS
7F	E8	+24	1-1	000	00	000			+24	R26	23.5	24.0	24.5	Adjustments are located on the power supply board.
7F	E8	FIXED +48	1-2	000	00	000			+48	R24	49.4	49.7	49.8	
7F	E8	SUPPLIES +5	1-3	000	00	000			+5	R18	5.05	5.1	5.15	See programmer manual.
7F	E8	-9	1-4	000	00	000			-9	R40	-8.8	-9.0	-9.2	See NOTE 1.
7F	E8	PROGRAMMABLE SUPPLY	1-5	000	00	000	7	1	PROG V		28.0		36.0	
7F	E8	VCC VERIFY LOW, V SET	2-1	001	01	001	5	1	TP3	R36	3.95	4.2	4.45	Set programmer in FWD. *Adjustment Step.*
7F	E8	VCC VERIFY HIGH, V SET	2-2	000	00	000	5	1	TP3	R38	5.75	6.0	6.25	Set programmer in REV. *Adjustment Step.*
7F	EC	VCC PROGRAM, V SET (1)	2-3	002	02	002	5	1	TP3	R37	5.25	5.5	5.75	*Adjustment Step.*
7F	EC	VCC CURRENT, ICC LIMIT	2-4	003	03	003	6	1	TP3		2.0		3.0	
7F	EC	VERIFY LOGIC LOW LEVEL	3-1	004	04	004	7	8	U6 P8		0.9		1.1	See NOTE 2. Set programmer in FWD. Test point located on analog card.
7F	EC	VERIFY LOGIC HIGH LEVEL	3-2	003	03	003	7	8	U6 P8		2.8		3.2	Set programmer in REV. Test point located on analog card.
7F	EC	BIT 8 VOL LOAD VERIFY	3-3	004	04	004	2	8	TP3		3.8		4.8	Set programmer in FWD.
7F	EC	BIT 8 VOH LOAD VERIFY	3-4	003	03	003	2	8	TP3		2.1		2.9	Set programmer in REV.
7F	EC	BIT 7 VOL LOAD VERIFY	3-5	004	04	004	2	9	TP3		3.8		4.8	Set programmer in FWD.
7F	EC	BIT 7 VOH LOAD VERIFY	3-6	003	03	003	2	9	TP3		2.1		2.9	Set programmer in REV.
7F	EC	BIT 6 VOL LOAD VERIFY	3-7	004	04	004	2	10	TP3		3.8		4.8	Set programmer in FWD.
7F	EC	BIT 6 VOH LOAD VERIFY	3-8	003	03	003	2	10	TP3		2.1		2.9	Set programmer in REV.
7F	EC	BIT 5 VOL LOAD VERIFY	3-9	004	04	004	2	11	TP3		3.8		4.8	Set programmer in FWD.
7F	EC	BIT 5 VOH LOAD VERIFY	3-10	003	03	003	2	11	TP3		2.1		2.9	Set programmer in REV.
7F	EC	BIT 4 VOL LOAD VERIFY	3-11	004	04	004	2	12	TP3		3.8		4.8	Set programmer in FWD.
7F	EC	BIT 4 VOH LOAD VERIFY	3-12	003	03	003	2	12	TP3		2.1		2.9	Set programmer in REV.
7F	EC	BIT 3 VOL LOAD VERIFY	3-13	004	04	004	2	23	TP3		3.8		4.8	Set programmer in FWD.
7F	EC	BIT 3 VOH LOAD VERIFY	3-14	003	03	003	2	23	TP3		2.1		2.9	Set programmer in REV.
7F	EC	BIT 2 VOL LOAD VERIFY	3-15	004	04	004	2	22	TP3		3.8		4.8	Set programmer in FWD.
7F	EC	BIT 2 VOH LOAD VERIFY	3-16	003	03	003	2	22	TP3		2.1		2.9	Set programmer in REV.
7F	EC	BIT 1 VOL LOAD VERIFY	3-17	004	04	004	2	21	TP3		3.8		4.8	Set programmer in FWD.
7F	EC	BIT 1 VOH LOAD VERIFY	3-18	003	03	003	2	21	TP3		2.1		2.9	Set programmer in REV.
7F	EC	$\overline{E2}$ PROGRAM, VPP LOW SET (2)	4-1	005	05	005	4	5	TP3	R34	26.0	27.0	28.0	*Adjustment Step.*
3D	EC	$\overline{E2}$ PROGRAM, VPP HIGH SET	4-2	006	06	006	4	5	TP3	R3	32.0	33.0	34.0	*Adjustment Step.*

COMMENTS
NOTES are on page 3.
Switch S1 must be depressed for accurate readings.
CAUTION: DO NOT LEAVE S1 DEPRESSED FOR EXTENDED PERIODS.

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	CALIBRATION CHART 017-1226-1 PAGE 2 OF 3
7D	EC	$\overline{E2}$ PROGRAM, VPP MEDIUM	4-3	007	07	007	4	5	TP3		29.0		31.0	
7D	EC	$\overline{E2}$ CURRENT, IPP LIMIT	4-4	007	07	007	6	5	TP3		2.5		3.5	CAUTION! See NOTE 2.
3D	ED	$\overline{E2}$ VERIFY	4-5	008	08	010	10	5	TP3		0.0		0.4	
3D	ED	E3 & E4 PROGRAM/VERIFY	4-6	008	08	010	7	6 & 7	TP3		5.0		5.15	2 Tests. See NOTE 1.
BD	E6	BIT 8 PROGRAM	5-1	009	09	011	3	8	TP3		25.0		27.0	
BD	E6	BIT CURRENT LIMIT	5-2	009	09	011	6	8	TP3		2.5		3.5	
BD	C6	BIT 8 DESELECT	5-3	010	0A	012	3	8	TP3		0.0		0.9	Confirm bit 8 ON (HEX 7F) on DO Bus.
BD	C6	BIT 7 PROGRAM	5-4	011	0B	013	3	9	TP3		25.0		27.0	
BD	A6	BIT 7 DESELECT	5-5	012	0C	014	3	9	TP3		0.0		0.9	Confirm bit 7 ON (HEX BF) on DO Bus.
BD	A6	BIT 6 PROGRAM	5-6	013	0D	015	3	10	TP3		25.0		27.0	
BD	86	BIT 6 DESELECT	5-7	014	0E	016	3	10	TP3		0.0		0.9	Confirm bit 6 ON (HEX DF) on DO Bus.
BD	86	BIT 5 PROGRAM	5-8	015	0F	017	3	11	TP3		25.0		27.0	
BD	66	BIT 5 DESELECT	5-9	016	10	020	3	11	TP3		0.0		0.9	Confirm bit 5 ON (HEX EF) on DO Bus.
BD	66	BIT 4 PROGRAM	5-10	017	11	021	3	12	TP3		25.0		27.0	
BD	46	BIT 4 DESELECT	5-11	018	12	022	3	12	TP3		0.0		0.9	Confirm bit 4 ON (HEX F7) on DO Bus.
BD	46	BIT 3 PROGRAM	5-12	019	13	023	3	23	TP3		25.0		27.0	
BD	26	BIT 3 DESELECT	5-13	020	14	024	3	23	TP3		0.0		0.9	Confirm bit 3 ON (HEX FB) on DO Bus.
BD	26	BIT 2 PROGRAM	5-14	021	15	025	3	22	TP3		25.0		27.0	
BD	06	BIT 2 DESELECT (4)	5-15	022	16	026	3	22	TP3		0.0		0.9	Confirm bit 2 ON (HEX FD) on DO Bus.
BD	06	BIT 1 PROGRAM (3)	5-16	023	17	027	3	21	TP3		25.0		27.0	
BD	26	BIT 1 DESELECT	5-17	024	18	030	3	21	TP3		0.0		0.9	Confirm bit 1 ON (HEX FE) on DO Bus.
3D	3C	PROGRAM V. KILL	5-18	025	19	031	4	5	TP3		0.0		0.4	
BD	C6	ADDRESS TEST VIL, A0 (5)	6-1	682	2AA	1252	7	20	TP3		0.0		0.4	
BD	C6	ADDRESS TEST VIH, A1	6-2	682	2AA	1252	7	19	TP3		4.8		5.15	
BD	C6	ADDRESS TEST VIL, A2	6-3	682	2AA	1252	7	18	TP3		0.0		0.4	
BD	C6	ADDRESS TEST VIH, A3	6-4	682	2AA	1252	7	17	TP3		4.8		5.15	
BD	C6	ADDRESS TEST VIL, A4	6-5	682	2AA	1252	7	16	TP3		0.0		0.4	
BD	C6	ADDRESS TEST VIH, A5	6-6	682	2AA	1252	7	15	TP3		4.8		5.15	
BD	C6	ADDRESS TEST VIL, A6	6-7	682	2AA	1252	7	14	TP3		0.0		0.4	
BD	C6	ADDRESS TEST VIH, A7	6-8	682	2AA	1252	7	13	TP3		4.8		5.15	
BD	C6	ADDRESS TEST VIL, A8	6-9	682	2AA	1252	7	2	TP3		0.0		0.4	

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
BD	C6	ADDRESS TEST VIH, A9	6-10	682	2AA	1252	7	3	TP3		4.8		5.15
BD	C6	ADDRESS TEST VIL, A10	6-11	682	2AA	1252	7	4	TP3		0.0		0.4
BD	26	ADDRESS TEST VIH, A0	6-12	1365	555	2525	7	20	TP3		4.8		5.15
BD	26	ADDRESS TEST VIL, A1	6-13	1365	555	2525	7	19	TP3		0.0		0.4
BD	26	ADDRESS TEST VIH, A2	6-14	1365	555	2525	7	18	TP3		4.8		5.15
BD	26	ADDRESS TEST VIL, A3	6-15	1365	555	2525	7	17	TP3		0.0		0.4
BD	26	ADDRESS TEST VIH, A4	6-16	1365	555	2525	7	16	TP3		4.8		5.15
BD	26	ADDRESS TEST VIL, A5	6-17	1365	555	2525	7	15	TP3		0.0		0.4
BD	26	ADDRESS TEST VIH, A6	6-18	1365	555	2525	7	14	TP3		4.8		5.15
BD	26	ADDRESS TEST VIL, A7	6-19	1365	555	2525	7	13	TP3		0.0		0.4
BD	26	ADDRESS TEST VIH, A8	6-20	1365	555	2525	7	2	TP3		4.8		5.15
BD	26	ADDRESS TEST VIL, A9	7-1	1365	555	2525	7	3	TP3		0.0		0.4
BD	26	ADDRESS TEST VIH, A10	7-2	1365	555	2525	7	4	TP3		4.8		5.15
BD	26	GROUND TEST	7-3	1365	555	2525	8	24	TP3		0.0		0.08
7F	AD	←—DATA PATTERN FOR ALL WORDS NOT SHOWN											

CALIBRATION CHART 017-1226-1

NOTES:

1: For the System 19, the limits for this test are .01 volt less than specified.
2. Do not hold S1 depressed for extended periods.

4.3.1 CHECK THE STATE OF THE START/STOP LINE

For steps that require confirmation of the state of the START/STOP line, perform the check as follows. To continue testing after confirming a STOP condition, START the programmer according to paragraph 4.3.2.

Models 1, 2, 3 and 5: Observe the START and STOP indicators.

Model 9: Press the PROM key and observe the data display. The programmer is in STOP if the display is blank; in START if the display shows data.

System 19: Observe the START light.

4.3.2 SET THE STATE OF THE START/STOP LINE

To set the state of the START/STOP line:

Models 1, 2, 3 and 5: Press the START/STOP key.

Model 9: Press KEYBOARD to STOP; press EXECUTE to START.

System 19: To set the START line high, with KEYBD selected and address and data displayed, depress the START key. Reselect KEYBD to STOP.

4.3.3 SET THE STATE OF THE FWD/REV LINE

To set the programmer in FORWARD or in REVERSE:

Models 1, 2, 3 and 5: Press the FWD key or the REV key.

Model 9: See MODEL 9 USERS NOTE, paragraph 4.3, to determine the right revision letter.

Revision "A" Software: Halt the programmer in FWD and in REV by entering data at an address and causing a mis-verify:

1. Ground J1-16 on the analog card.
2. Press LOAD.
3. Press EXECUTE.
4. Press KEYBOARD.
5. Key in data – Ø1 hex – at address ØØ1.
6. Press VERIFY.
7. Press EXECUTE. The programmer will mis-verify at the address containing data and will STOP in FWD.
8. Press SKIP. The programmer will mis-verify at the address containing data and will halt in REV.

Revision "B" or later Software: Press the FWD key to set the programmer in FORWARD and the REV key to set it in REVERSE.

System 19: With KEYBD selected, press ENTER to set the programmer in FORWARD and REVIEW to set it in REVERSE.

4.3.4 LOAD DATA ONTO THE DI BUS

The data on the calibration chart is to be loaded on the DI bus using the programmer keyboard.

Models 1, 2 and 5: Key in binary data called out on the Calibration Chart. (Bits called out must be ON, bits not called out must be OFF.) Perform the necessary number-system conversions if using an octal or hexadecimal keyboard. Confirm correct data by checking the binary DI display.

Model 3: Use an external source, such as a paper tape reader, to put binary data on the DI bus.

Model 9: (See MODEL 9 USERS NOTE, paragraph 4.3, to determine the correct revision letter.) When using a Model 9, always key in the hex data in parentheses to be sure that the correct data is placed on the DI bus.

Revision "A" Software:

Halt the programmer in the automatic program mode with data on the DI bus.

1. Clear RAM: Select INVERT. Then press and hold the EDIT key while pressing LOAD.
2. Press the KEYBOARD key, and key in hex data called out in parentheses on the calibration chart.
3. Press the PROGRAM key.
4. Ground J1-16 on the analog card.
5. Press EXECUTE and wait for the programmer to abort.
6. Press STOP, KEYBOARD and EXECUTE.
7. Disconnect J1-16 from ground.
8. SET the address specified on the calibration chart in order to make the measurement.

Revision "B" or later Software:

1. With the EXECUTE indicator illuminated and all the others OFF, use the hex keypad to key in hex data called out in parentheses on the calibration chart.

System 19:

Key the hex data in parentheses into RAM at the specified address. The data and address shown in the display are present on the DI bus.

4.3.5 CONFIRM DATA ON THE DO BUS

To view DO Bus data:

Models 1, 2, 3 and 5: Compare the bit callout on the calibration chart with the OUTPUT DATA display on the programmer front panel. Bits not called out must be OFF.

Model 9: Press the PROM key and observe the data display on the programmer front panel. Data must match the hex callouts on the calibration chart.

System 19: With KEYBD selected, press the DEVICE DATA key.

4.4 WAVEFORM OBSERVATION

Programming waveforms should be observed after complete DC calibration of the programmer and Program Card Set. Set-up instructions assume that the calibration equipment is already installed for calibration per paragraph 4.2.

In waveform observation, oscilloscope displays are to be compared with the Timing Diagram. These waveforms, indicated by circled digits on the timing diagram, are indentically referenced on the Calibration Chart. Waveforms are selected using switches S2 and S3 on the Universal Calibrator as specified on the Calibration Chart.

4.4.1 CALIBRATION EQUIPMENT SET-UP

Refer to Figure 4-5.

1. Make sure that the programmer power is OFF.
2. Remove the digital card from the card slot.
3. Check the timing diagram to determine the number of the reject jumper. Find and remove the jumper on the digital card (if installed), making sure to note the position in which it is installed.

CAUTION

Be sure to replace the reject (abort) jumper (if it was installed) in the proper position after waveform observation.

4. Disconnect the 16-conductor cable at J1 of the Universal Calibrator.
5. Connect the free end of the 16-conductor cable to digital card J1, making sure that the red cable stripe and pin 1 are properly oriented.
6. Connect the triggered input of a dual-trace oscilloscope to the digital-card test point as indicated to the left of the TEST waveform on the timing diagram. Connect an input probe to TP3 on the calibrator.
7. Reinstall the digital card in the slot from which it was removed.

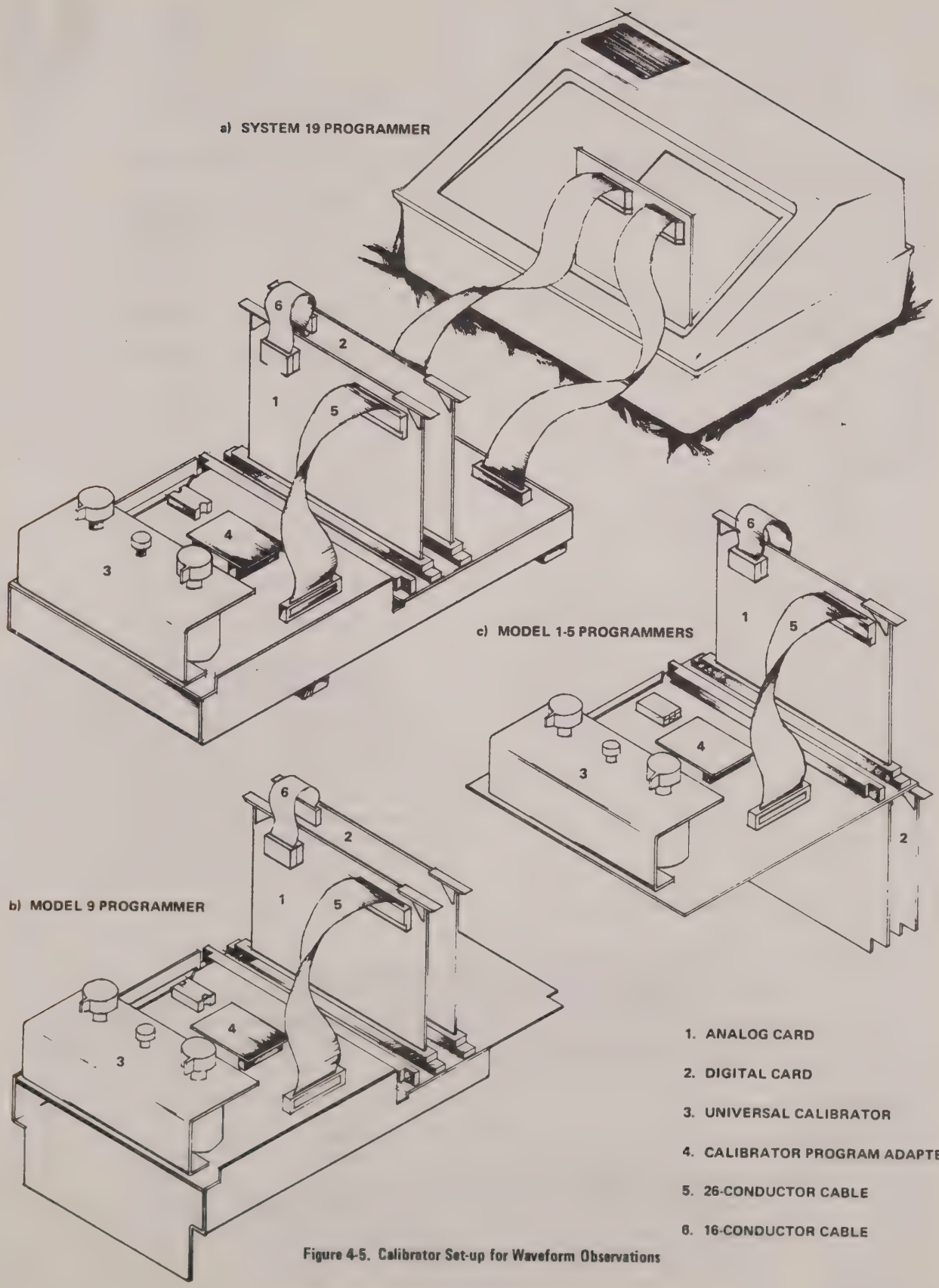


Figure 4-5. Calibrator Set-up for Waveform Observations

8. Check the NOTES column of the timing diagram to determine whether the Program Card Set defaults to VOH or VOL for calibration. If and only if the card set defaults to VOH, ground J1-16 (Read Enable line) to the GND test point on the Universal Calibrator.

CAUTION

Do not connect J1-16 to any other potential; damage to programmer components may result.

4.4.2 TEST PROCEDURE

Observing programming waveforms requires putting data in RAM and causing the programmer to attempt to program a nonexistent device.

1. Turn programmer power ON.

2. Prepare the programmer for keyboard data entry.

Models 1 – 5, press: RESET
RAM-RAM
PROGRAM
MANUAL
START

Model 9: Set the NORMAL/INVERT switch in NORMAL if the Program Card Set is calibrated VOH or in the INVERT position if VOL. The NOTES column on the timing diagram specifies the correct polarity. Press: KEYBOARD.

System 19 press: KEYBD
Ø
ENTER

3. Key in data for bit 1 at several addresses:

Models 1 – 5: Enter bit 1 at several addresses and confirm that bit 1 is ON and all other bits are OFF on the DI display.

Model 9: Enter hex data "Ø1" at several addresses.

System 19: Enter hex data at several addresses. Check the NOTES column on the Timing Diagram to determine the correct data polarity. If the timing diagram indicates VOH, enter a hex "1". If the timing diagram indicates VOL, enter a hex "E" for 4-bit card sets; "FE" for 8-bit card sets.

4. Select the PROGRAM mode:

Models 1 – 5, press: RESET
PROGRAM
AUTO
RAM-ROM2

Model 9, press: PROGRAM

System 19, press: SELECT
CØ
START
PROG

5. Initiate waveforms:

Models 1 – 5, press: START

Model 9, press: EXECUTE

System 19, press: START

After initiating the programming sequence, the programmer will halt at the first address which has data. Refer to the timing diagram and calibration chart by the circled digits (①, ②, ③,...). Make the indicated switch selections with S2 and S3 on the Universal Calibrator.

Observe specific waveforms relative to the triggered test pulse by pressing S1 on the calibrator. S3 is used to route analog card output to TP3 (the oscilloscope probe); S2 selects resistive loads that are applied when S1 is pressed. All other information on the calibration charts is of no importance during waveform observation.

CAUTION

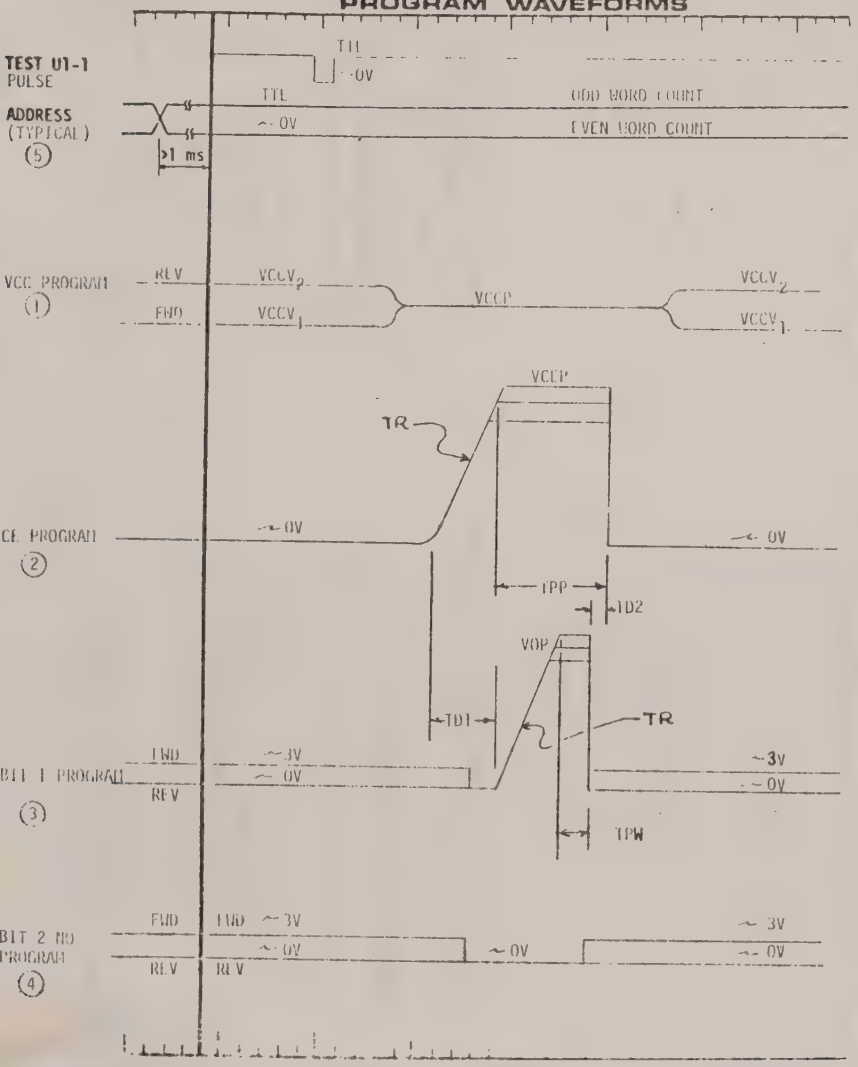
When S1 is depressed high currents are induced within the programmer; do not hold S1 depressed for extended periods.

6. Stop programming:

Models 1 – 5 and 9, Press: STOP

System 19, press: KEYBD

PROGRAM WAVEFORMS



NOTES

For calibration, the card set polarity defaults to Vol.

DIGITAL CARD JUMPERS - 1225

- JP1 = OPEN
- JP2 = SHORT
- JP3 = SHORT
- JP4 = SHORT
- JP5 = SHORT
- JP6 = OPEN
- JP7C = 9 PULSE REJECT
- JP7M = 1 PULSE REJECT
- JP8 = OPEN
- JP9 = N
- JP10 = WORD LIMIT = 2048
- JP11 = SHORT

ABORT TIMER = JP1 - NOT USED

PAUSE TIMER (CR2) = NOT USED

WAVEFORM VARIABLES

- TPP = 30 μSEC ≤ TPP ≤ 100 μSEC
- TR = .4V/μSEC ±15%
- TD1 ≥ 10 μSEC
- TD2 ≥ 100 n sec
- TPW = 7 ± 5 u sec
- $VCCV_1$ = 4.2 ± .25V
- $VCCV_2$ = 6.0 ± .25V
- VCCP = 5.5 + 0.25 V

NOTE: TR ADJUST FOR BIT 1 PROGRAM = ANALOG R39

PULSE NO.	VCEP*	VOP*
1 - 3	27	20
4 - 6	30	23
7 - 9	33	26

* ± 1.0V Tolerance

These waveforms correspond to callouts on the Calibration Chart. Switch S2 of the Universal Calib. to indicated positions to obtain waveforms. Refer to Performance Check section of manual for detailed steps.

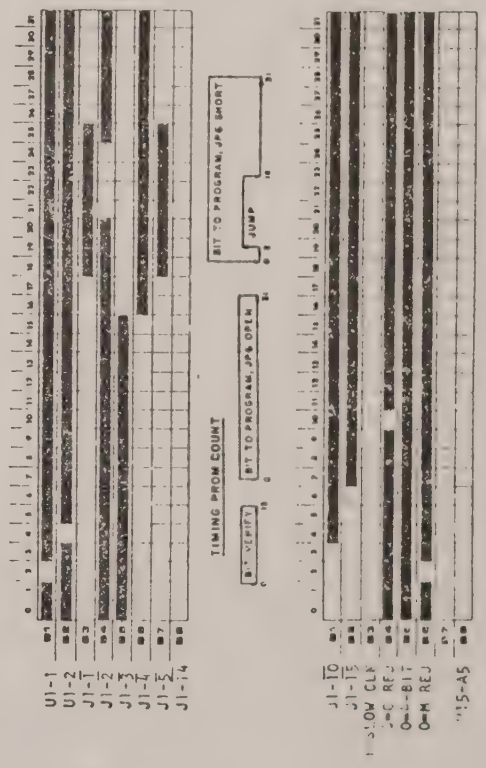
DATE	SYM	REVISION RECORD	DR	CK
1-75		CN 610	LC	EL
7-75	1	CN 1071	RT	LJ
3-77	D	CN # 1125	DS	KF
9-77	-	CORRECTED Vcc PROG. NOM	DP	DF

TRUTH TABLES

LINE : HI(1), NO LINE : LOW(Ø)

TIMING ROM U1

MODE ROM U15



DATA I/O

TIMING DIAGRAM

M.M.I. GENERIC

12-1-75

007-1226-1

4.4.3 REJECT JUMPER REINSTALLATION AND ABORT TEST

Before putting the Program Card Set back in use, it is necessary to reinstall the reject (abort) jumper and confirm the operation of the abort function on the digital card.

1. Turn the programmer power OFF.
2. Remove the digital card from the card slot.
3. Refer to the Timing Diagram for the reject jumper. number and make sure to install the jumper in the position from which it was removed.
4. Reinstall the digital card in the card slot.
5. Repeat the key sequence in Waveform Test Procedure, paragraph 4.4.2, steps 1-5.
6. With Universal Calibrator switch positions selected to observe the test pulse waveform, repeat step 6 of the Test Procedure. Note with the oscilloscope that the waveform display is terminated by the programmer. This indicates that the abort function of the digital card is operative.

SECTION 5

CIRCUIT DESCRIPTION

5.1 INTRODUCTION

The Data I/O Program Card Set consists of a digital card, an analog card, and interconnecting cables. Both cards interface with the programmer and with each other. The analog card interfaces with the device being programmed or read. Figure 5-1 gives a generalized block diagram of the relations among the cards, the programmer, and the device.

5.1.1 DIGITAL CARD

The digital card receives data from the programmer on the DI bus, and from the device on the DO bus. The data on these busses are compared at each bit both before and after programming. At each bit, the digital card continues to command program pulses from the analog card until the bit is programmed unless an ABORT or REJECT is signalled.

5.1.2 ANALOG CARD

The analog card receives bit and word addresses, timing and mode commands. In turn, the analog card supplies programming signals of voltages and currents specified by the device manufacturer. When recommended by the manufacturer, each programmed bit is tested for loading and/or leakage. The analog card reads the device, once it is programmed, to verify that programmed data matches truth-table data.

5.1.3 DETAILED CIRCUIT DESCRIPTION

The following paragraphs explain the functions of the digital card and analog card.

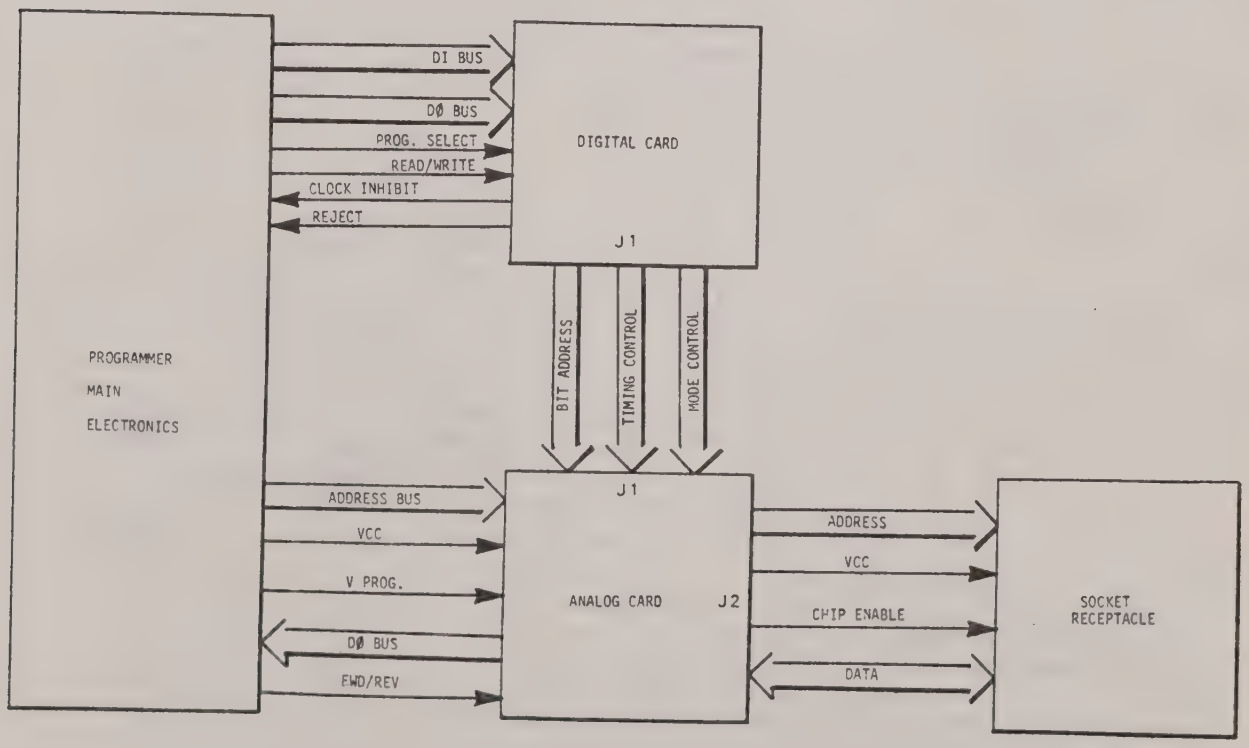


Figure 5–1. Simplified Block Diagram of Program Card Set

5.2 DIGITAL CARD

5.2.1 BLOCK DIAGRAM

Figure 5-2 gives a generalized block diagram of the digital card This diagram shows signal flow and functional relationships between the blocks but does not include detailed interconnect information. Refer to the schematics and timing diagram (with truth tables) for details of circuit connection and operation. The following paragraphs discuss the functions performed by the digital card.

5.2.2 PROGRAM MEMORY

When the digital card is selected for operation, the Program Memory will set upon receiving a Write command on AA. This causes the Clock Generator on the digital card to begin operation and halts the programmer clock. Initialization of the Program Pulse Counter, Bit Counter and Sequence Counter and clearing of the Over-program Counter occur before the Program Memory is set.

5.2.3 CLOCK GENERATOR

When the Program Memory toggles in response to the Write and Program Select commands, the Clock Generator begins operation and the programmer clock is inhibited. Clock pulses increment the Sequence Generator. The clock rate is determined by the Mode and Timing PROM or by High Order Memory (with JP8 connected). The Clock may be halted by the Abort Timer or by the Pause Timer (with CR2 connected).

5.2.4 THE SEQUENCE COUNTER AND TIMING PROM

The Sequence Generator consists of a 4-bit counter which drives the 32x8 Timing PROM. The combination generates timing signals for analog control, along with Bit Test and Bit Increment pulses, which are used on the digital card. (See the Timing Diagram.) A clock pulse is also output for PROMs with registers.

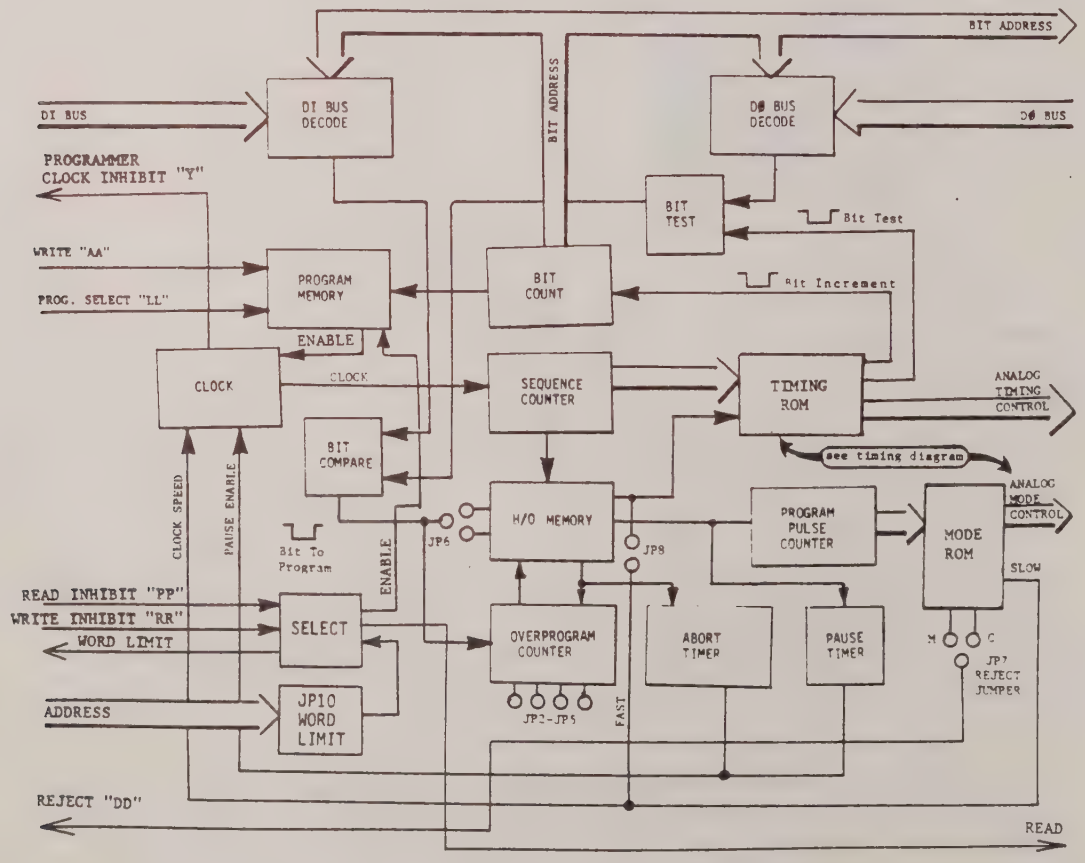


Figure 5–2. Block Diagram, 1225 Digital Card

5.2.5 BIT COUNTER

The Bit Counter counts Bit Increment pulses arriving from the Timing ROM. Bit Increment pulses are counted, however, only when H/O Memory is enabled via a Bit to Program pulse from the Bit Compare gate. The Bit Counter counts down from either 4 or 8, as determined by input from the analog card or from the Mode PROM. Output from the Bit Counter controls the DO Bus Decoder and DI Bus Decoder. When the Bit Counter reaches zero, its borrow output is used to reset the Program Memory.

5.2.6 PROGRAM PULSE COUNT AND MODE CONTROL

As program pulses are delivered to the PROM being programmed, the Program Pulse Counter counts up; outputs from the Program Pulse Counter are used as address line inputs to the Mode Control PROM. The Timing diagram includes the truth table for the Mode Control PROM. Outputs of Mode ROM control the magnitude of program pulses (bits 1 and 2), along with clock speed (bit 3). Bits 4 and 5 control the number of programming attempts allowed before a reject is returned to the programmer; reject jumper JP7 selects either the M line or the C line. (See the Timing Diagram for the pulse numbers selected.)

5.2.7 TIMING PROM

Output words from the Timing PROM are used in the serial Verify and Program operations, as shown in the Timing Diagram. Verify operations use Low Order words 0 to 15; Program operations use High Order words 16 through 31. Words 8 through 11 are used to output control for VCC voltages during Read and Verify operations. These operations occur under machine control when the digital card is not selected. At the beginning of a programming sequence (word 2), the Timing PROM outputs a Bit Test pulse to the Bit Test gate. If the DO Bus Decoder determines that there is no bit already programmed in the PROM, and if the DI Bus Decoder determines that there is a bit to program, then the Compare Gate outputs a Bit to Program pulse.

5.2.8 OVERPROGRAM COUNTER

The Bit to Program pulse arrives at the preset input of the H/O Memory and at the load port of the Overprogram Counter. As H/O Memory is preset, the Bit Count Gate is disabled and remains so until the Overprogram Counter clocks H/O Memory after the bit has been programmed.

At H/O Memory Word 15, the carry pulse from the Sequence Counter, is allowed to toggle U13B. (See Schematic.) As U16B is toggled the fifth address line to the Timing PROM is enabled, and it advances into High Order (Program) Count, words 16 through 31.

At word count 31, the Sequence Counter outputs another carry pulse to H/O Memory. The carry pulse toggles U13B which sets the Timing ROM back to Low Order Count (Verify). At word 2, again, a Bit Test pulse is output from the Timing PROM; if the buses compare at Bit Test (bit is programmed), the output of Bit Compare gate remains unchanged (no Bit to Program), the H/O Memory remains enabled, and the Bit Count gate remains disabled.

At word 15 the Sequence Counter outputs another carry pulse which again causes a High Order (Program) count, causing the Overprogram Counter to decrement. The above cycle repeats until the Overprogram Counter outputs a borrow pulse after counting down from the level preset by JP2—JP5. The borrow pulse clocks H/O Memory which enables the Bit Count gate, allowing it to decrement the Bit Count to the next bit.

Some digital cards are wired with JP6 shorted. If JP6 is shorted Program Memory holds H/O Memory reset so that the Timing PROM jumps to High Order (Program Cycle) after Bit Test. When a Bit to Program pulse is received at (shorted) JP6, the fifth address input line to the Timing PROM goes high and H/O Memory is enabled. At Word 31, the carry pulse from the Sequence Counter shifts the count sequence back to Low Order. With JP6 shorted, the total sequence is 16 clock pulses long.

5.2.9 ABORT TIMER

The Abort Timer measures the time required to program a bit. If programming time is excessive, and JP1 is shorted, a REJECT is signaled and the clock is halted. The Abort Timer is connected to the Overprogram Counter such that an abort is possible only during Low Order count (Verify cycle).

5.2.10 PAUSE TIMER

The Pause Timer measures the time to program the PROM. A transistor is used in conjuction with the timing components to integrate out the time that the Program Memory is set. If programming time exceeds the value set by circuit components, the Clock is stopped in order to allow the PROM to cool; after a pause in the order of seconds the Clock is allowed to start again, and programming continues. Pause Timer output is gated with the Timing PROM so that a pause cannot occur during program pulses.

5.2.11 SELECT GATES

U17 and U18 (on schematic) monitor Program Select (LL), Write Inhibit (PP), Read (X), and Read Inhibit (RR) in order to enable operation of the digital card. Output from Read Gate U17 is routed to the analog card to control the Data Bus Drivers.

5.2.12 WORD LIMIT SELECT

Word Limit is jumper–selected at JP10 on the digital card to 32, 64, 256, 512, 1024, or 2048. JP10 limits the address range of the programmer through the Word Limit line (CC), according to the configuration of the PROM being programmed.

5.3 ANALOG CARD

5.3.1 BLOCK DIAGRAM

Refer to Figure 5–3 for functions and signal flow of the analog card.

5.3.2 BIT DECODE

PROM bits are programmed individually within a given PROM work. Bit information in BCD form arrives at analog card J1 and is used to drive the BCD to decimal Bit Decoder. Decoder outputs enable appropriate Bit Program Switches to transfer program pulses to the bit lines of the PROM being programmed.

During clock periods 21–24 of the program cycle the Bit Switches are turned ON, allowing the output of the Program Voltage Generator to reach the PROM bit lines.

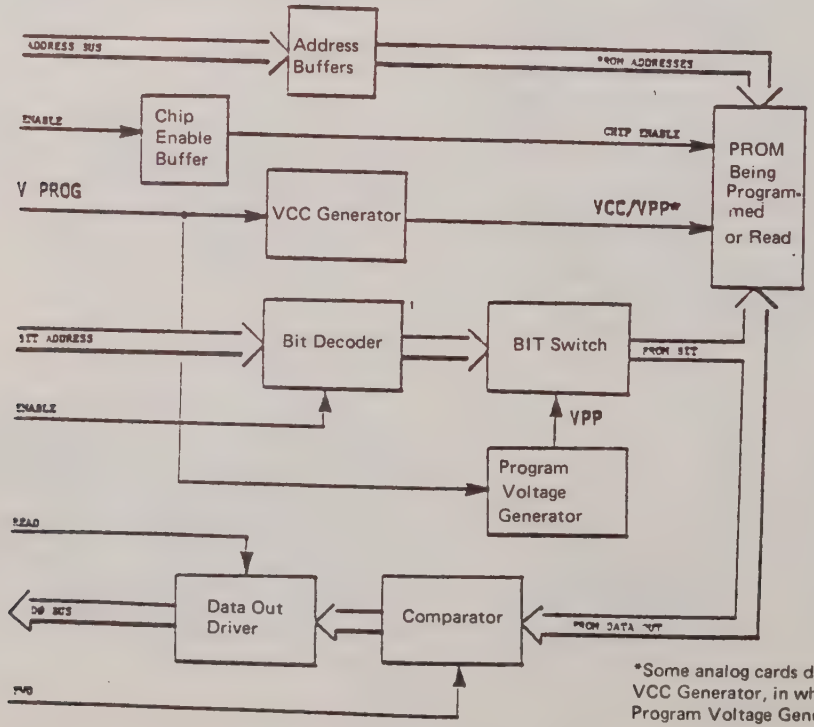
5.3.3 PROGRAM VOLTAGE GENERATOR

During the initial portion of the program cycle (period 18) the Program Voltage Generator is switched ON. The Program Voltage Generator output is routed to the PROM.

The Program Voltage Generator receives voltage increment inputs from the digital card Mode Control PROM. As the programmer attempts to program the PROM, increasingly higher program voltages are used. (See the Timing Diagram.) The magnitude of Program voltages (High and Low) are set by calibration resistors.

5.3.4 RAMP GENERATOR

The Ramp Generator consists of a current limiter and an emitter follower. The emitter follower provides voltage to the Bit Switches during clock periods 21–24, allowing output from the Program Voltage Generator to reach the PROM bit being programmed.



*Some analog cards derive VPP from the VCC Generator, in which case the VPP Program Voltage Generator may be omitted.

Figure 5–3. Block Diagram, 1226–1 Analog Card

5.3.5 VCC GENERATOR

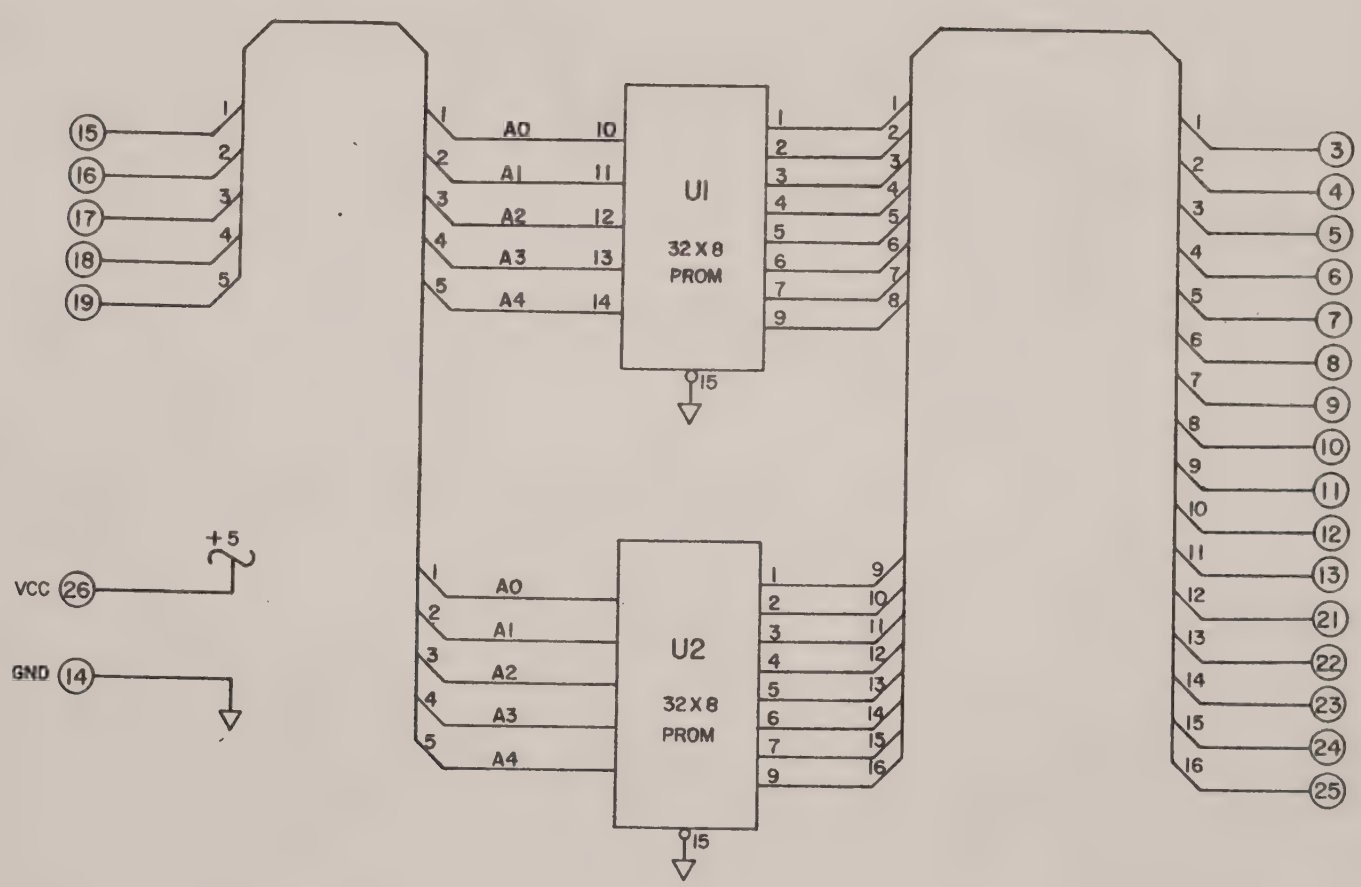
The VCC Generator outputs three voltages; VCC Program, VCC low, and VCC High. During the program cycle, VCC is set at VCC Program, as determined by the setting of a calibration resistor. When the programmer is in FWD, VCC is nominally set at VCC Low, as determined by another calibration resistor. With the programmer in REV, VCC Generator output is at VCC High. Refer to the Timing Diagram for details on voltage levels; see Calibration section for adjustment information.

5.3.6 COMPARATORS

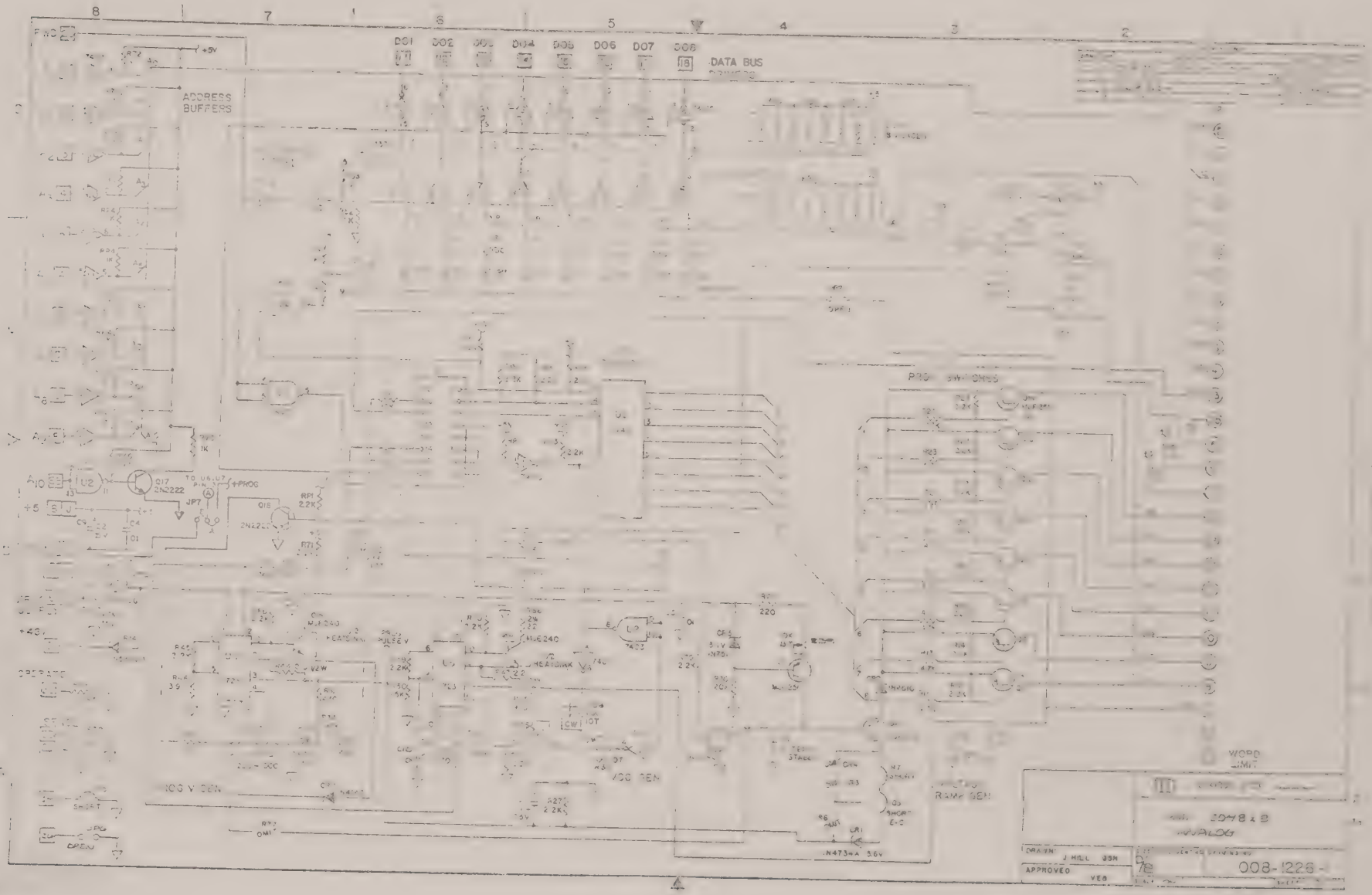
PROM output is tested during Verify and Read for VOL in FWD and for VOH in REV. In FWD, a load switch connects load resistors to PROM output bits. Current through these resistors develop voltages at the + inputs of the comparators. Positive input is compared with negative input from a reference level generator. If the levels compare (bit is programmed) the information is transferred to the digital card through the DO Bus.

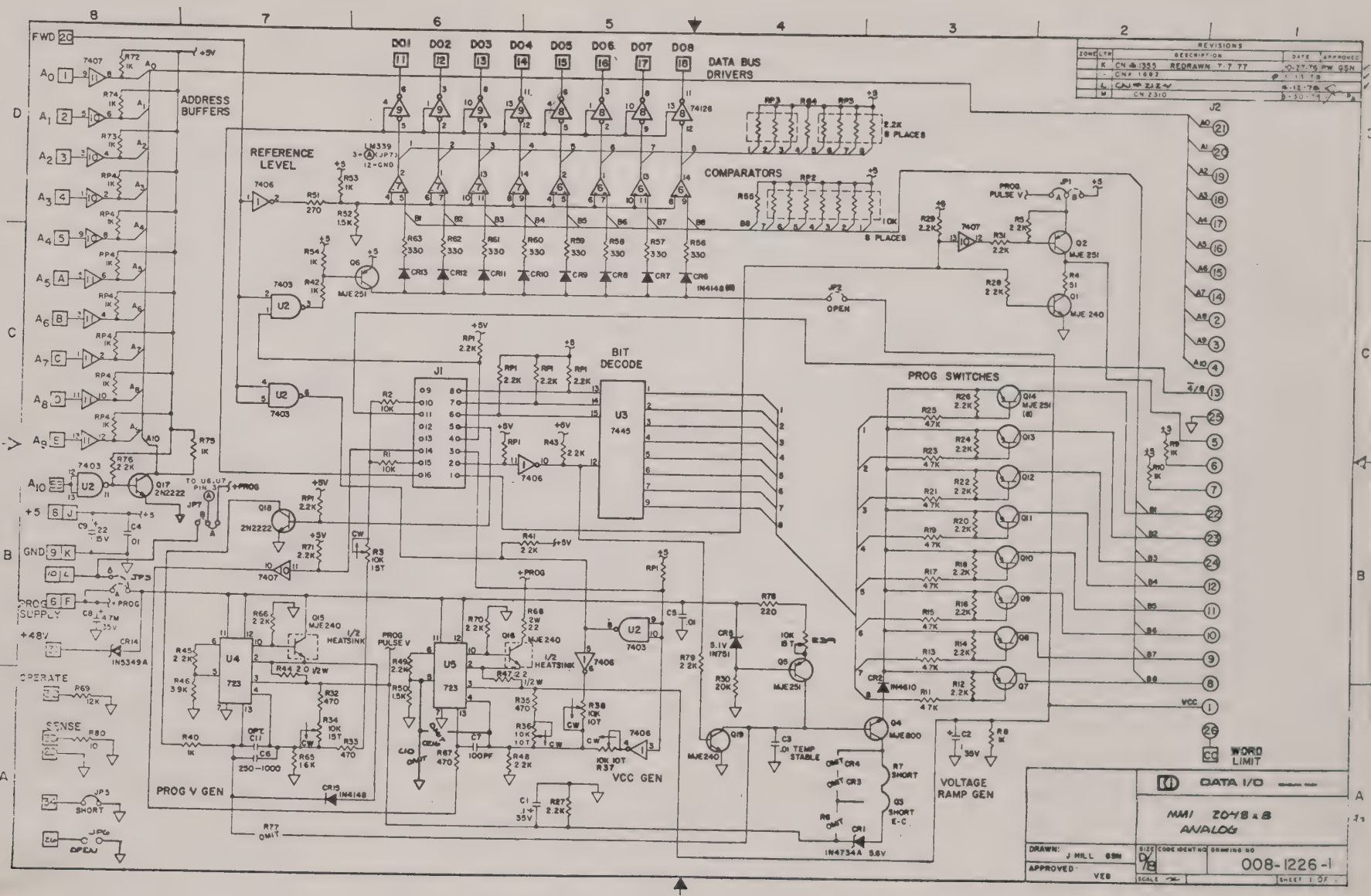
In REV, the situation is similar, but PROM VOH levels are tested, and the reference level generator outputs a higher voltage to the negative inputs of the Comparator.

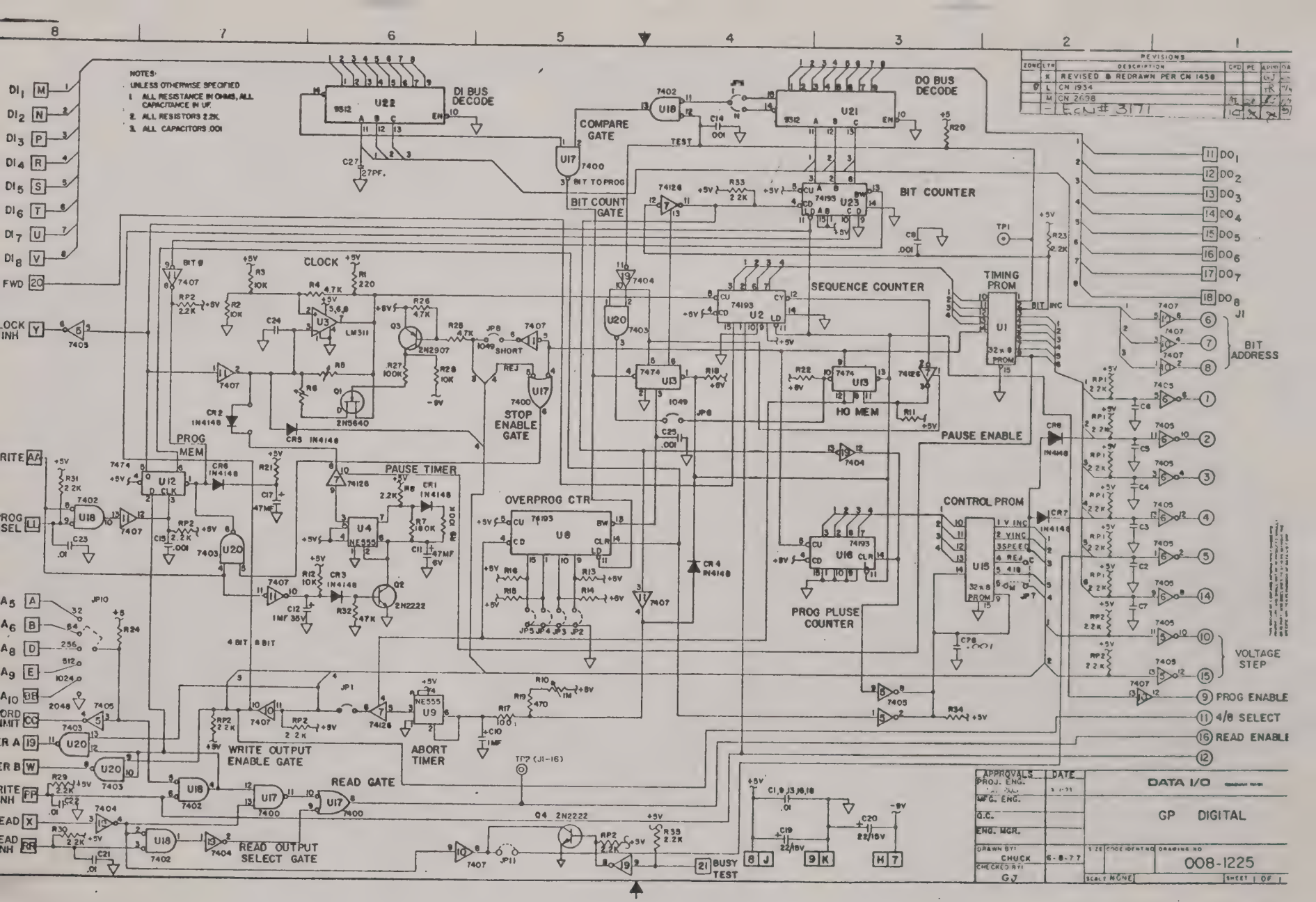
DATE	SYM	REVISION RECORD	DR	CK
11-13-75	A	RELEASE		



TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH		
DECIMAL -		SCALE	DRAWN BY G. ROPPE
FRACTIONAL -	TITLE PLUG IN ADAPTER (UNIVERSAL CALIBRATOR)		APPROVED BY
ANGULAR -	DATE 10-15-75	DRAWING NUMBER 008-1072	


ADDRESS BUFFERS
DATA BUS
+5V
Q17 2N2222
Q16 2N2222
+PROG
JP7
RP1 2.2K
R71
MJE240
HEATSINK
100 V GEN
VCC GEN
RAMP GEN
WORD LIMIT
ANALOG
DRAWN J HILL 83M
APPROVED VEB
008-1228-


DATA BUS DRIVERS
ADDRESS BUFFERS
REFERENCE LEVEL
COMPARATORS
BIT DECODE
PROG SWITCHES
PROG V GEN
VCC GEN
VOLTAGE RAMP GEN
PROG SUPPLY
SENSE
OPERATE
WORD LIMIT
DATA I/O
MMI 2048 A & B
ANALOG
008-1226-1


NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE IN OHMS, ALL CAPACITANCE IN UF.
2. ALL RESISTORS 2.2K
3. ALL CAPACITORS .001
DI BUS DECODE
DO BUS DECODE
COMPARE GATE
BIT COUNT GATE
BIT COUNTER
CLOCK
SEQUENCE COUNTER
TIMING PROM
BIT ADDRESS
STOP ENABLE GATE
PROG MEM
PAUSE TIMER
HO MEM
PAUSE ENABLE
OVERPROG CTR
CONTROL PROM
PROG PLUSE COUNTER
VOLTAGE STEP
WRITE OUTPUT ENABLE GATE
ABORT TIMER
READ GATE
READ OUTPUT SELECT GATE
PROG ENABLE
4/8 SELECT
READ ENABLE
BUSY TEST
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